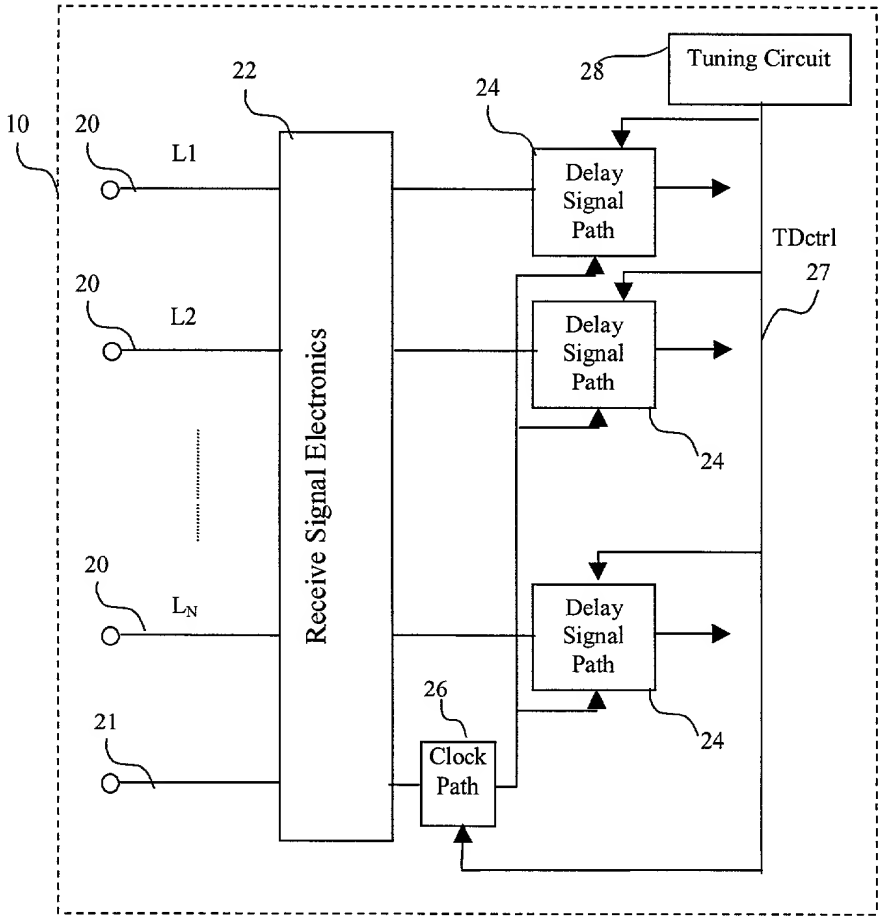

10
20
L1
22
24
28
Tuning Circuit
Delay Signal Path
TDctrl
27
20
L2
Receive Signal Electronics
Delay Signal Path
24
20
L_N
Delay Signal Path
24
21
26
Clock Path

FIG 1

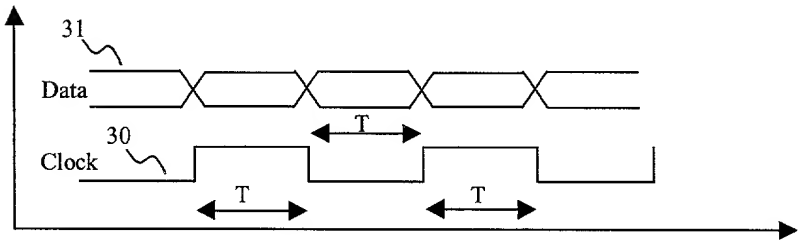

31
Data
T
30
Clock
T
T

FIG 2

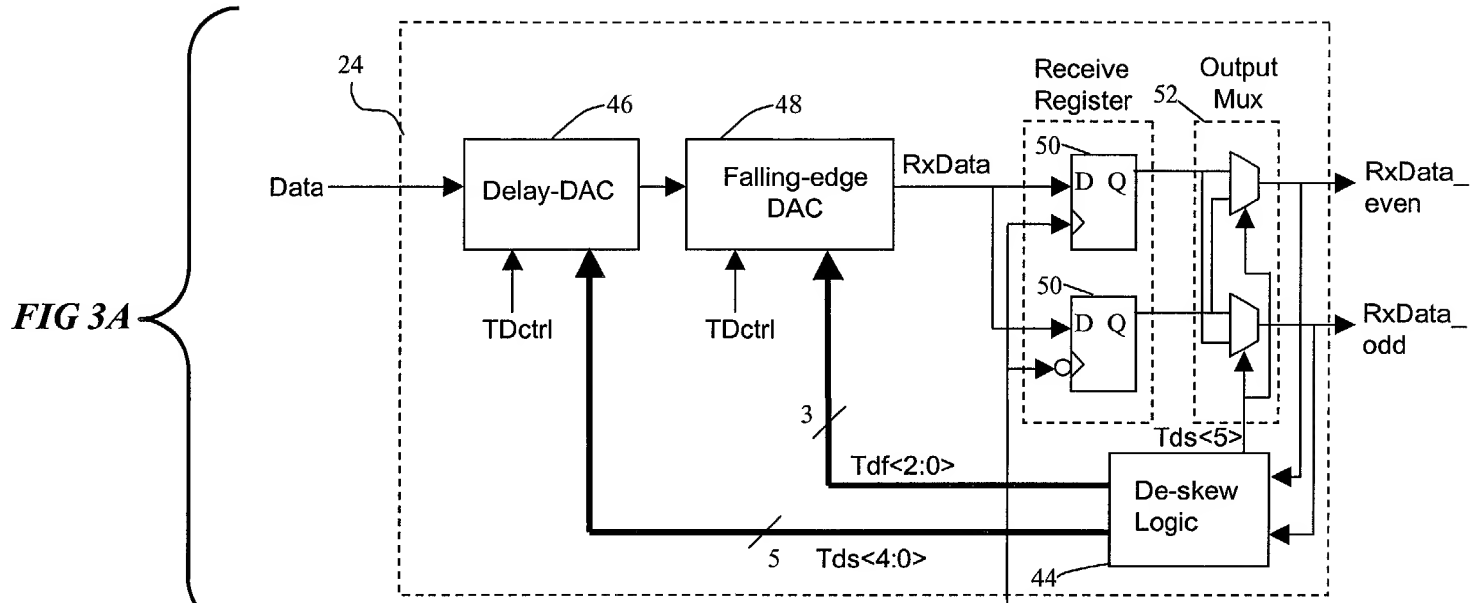

24
46
48
Receive Register
Output Mux
52
Data
Delay-DAC
Falling-edge DAC
RxData
50
D Q
RxData_ even
50
D Q
RxData_ odd
TDctrl
TDctrl
3
Tdf<2:0>
Tds<5>
De-skew Logic
5
Tds<4:0>
44

FIG 3A

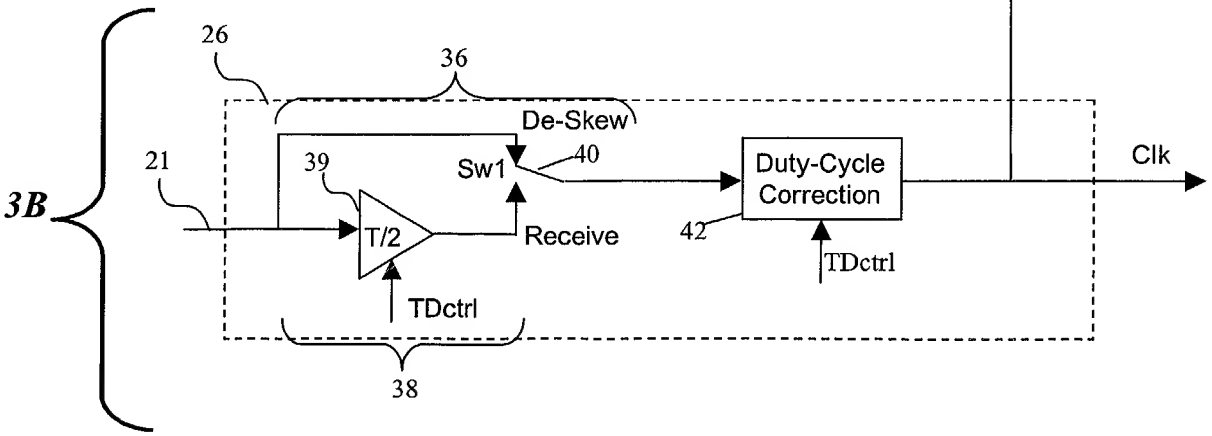

26
36
De-Skew
21
39
Sw1
40
Duty-Cycle Correction
Clk
T/2
Receive
42
TDctrl
TDctrl
38

FIG 3B

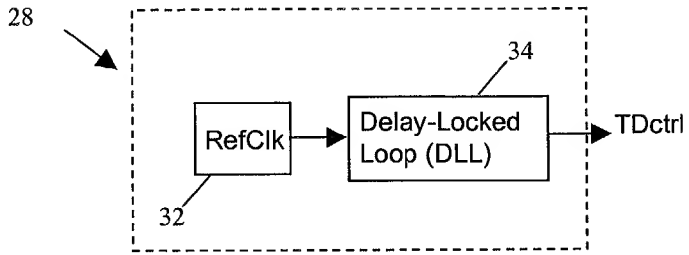

28
34
RefClk
Delay-Locked Loop (DLL)
TDctrl
32

FIG 3C

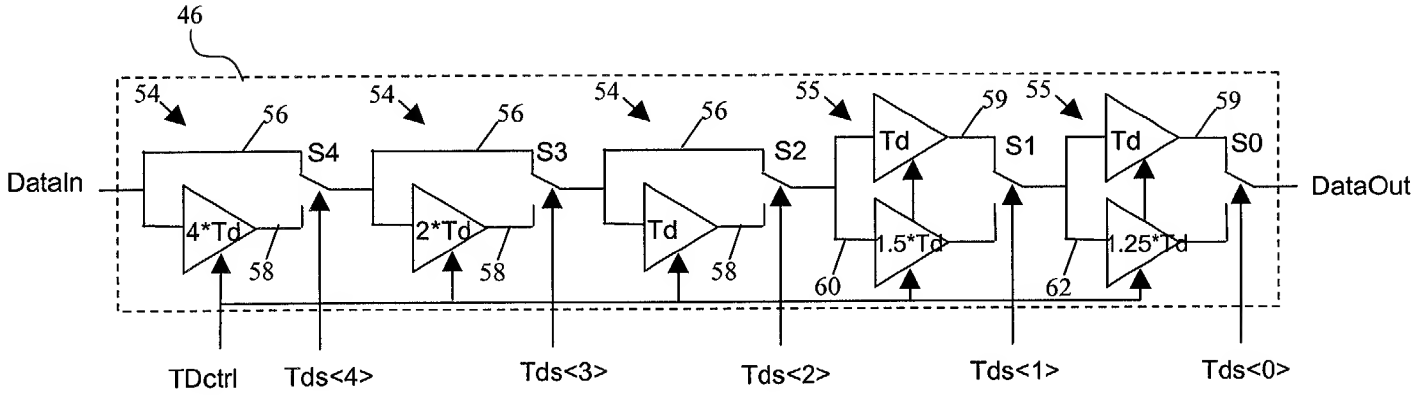

46
54
56
S4
54
56
S3
54
56
S2
55
59
Td
S1
55
59
Td
S0
DataIn
DataOut
4*Td
58
2*Td
58
Td
58
1.5*Td
60
1.25*Td
62
TDctrl
Tds<4>
Tds<3>
Tds<2>
Tds<1>
Tds<0>

FIG 4

FIG 5A

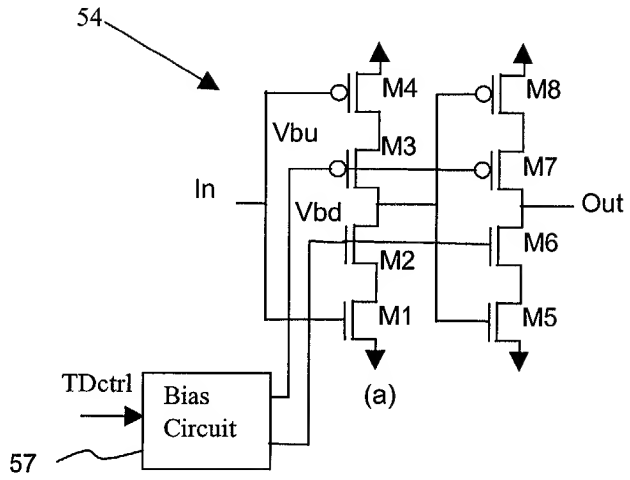
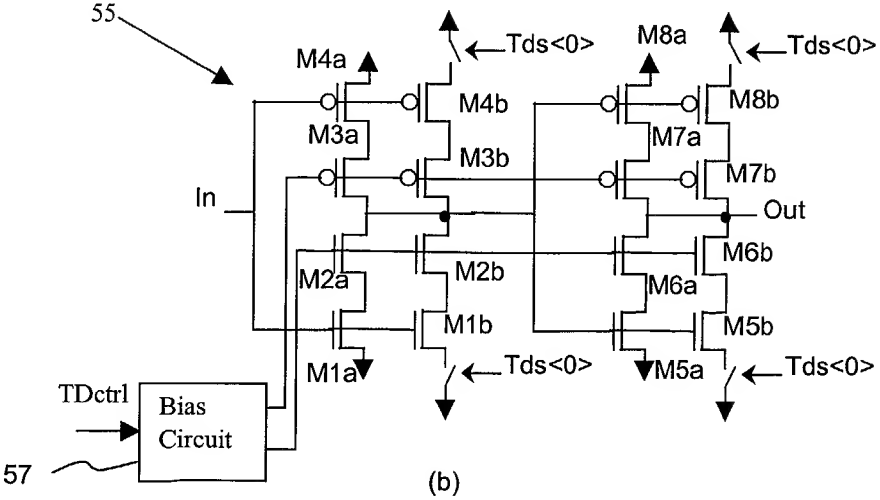

54
M4
M8
Vbu
M3
M7
In
Vbd
Out
M6
M2
M1
M5
TDctrl
Bias
Circuit
57
(a)

FIG 5B


55
M4a
Tds<0>
M8a
Tds<0>
M4b
M8b
M3a
M7a
M3b
M7b
In
Out
M6b
M2a
M2b
M6a
M1b
M5b
M1a
Tds<0>
M5a
Tds<0>
TDctrl
Bias
Circuit
57
(b)

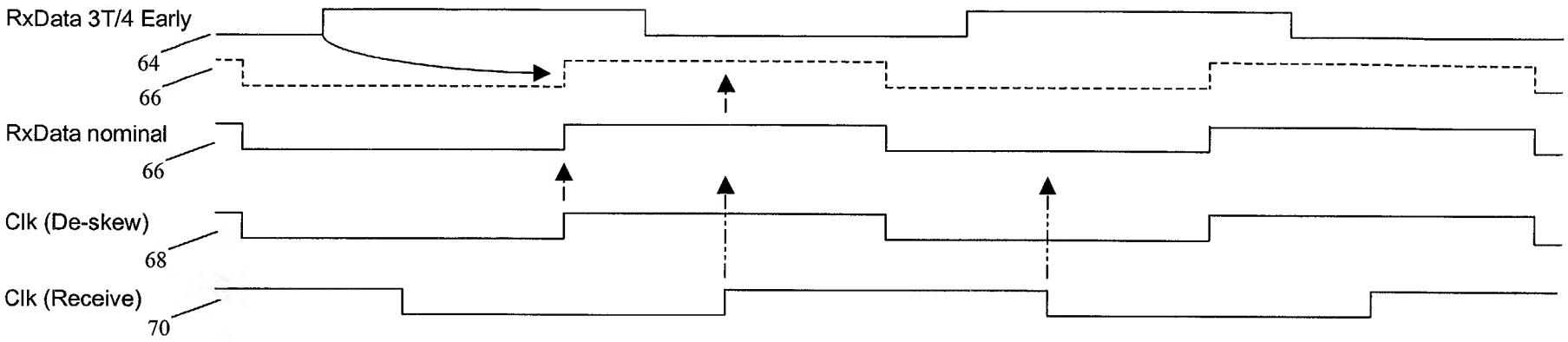

RxData 3T/4 Early
64
66
RxData nominal
66
Clk (De-skew)
68
Clk (Receive)
70

FIG 6A

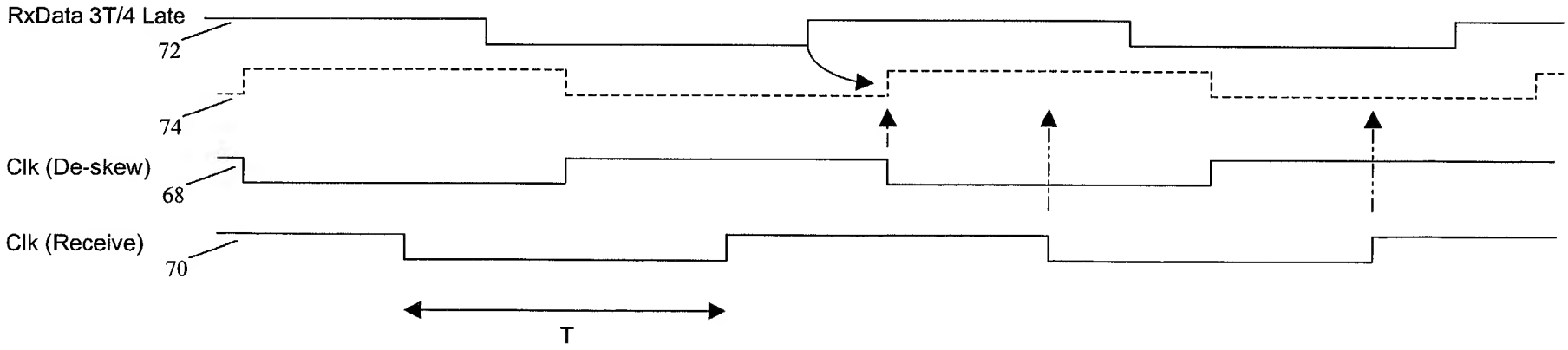

RxData 3T/4 Late
72
74
Clk (De-skew)
68
Clk (Receive)
70
T

FIG 6B

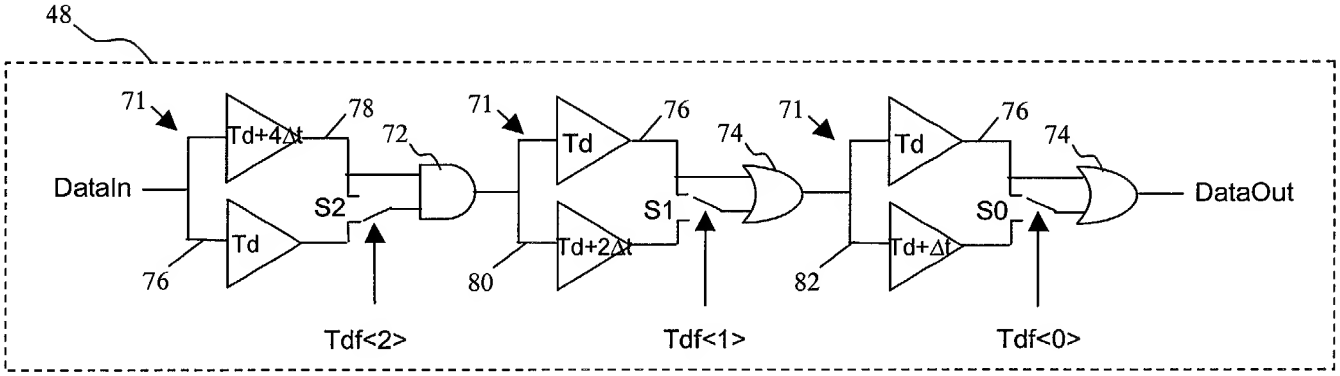

48
71
Td+4Δt
78
72
71
Td
76
74
71
Td
76
74
DataIn
S2
S1
S0
DataOut
Td
76
Td+2Δt
80
Td+Δt
82
Tdf<2>
Tdf<1>
Tdf<0>

FIG 7

Tdf<2>,Tdf<1>,Tdf<0>	Falling Edge Delay
0,0,0	3Td
0,0,1	3Td+Δt
0,1,0	3Td+2Δt
0,1,1	3Td+3Δt
1,0,0	3Td+4Δt
1,0,1	3Td+5Δt
1,1,0	3Td+6Δt
1,1,1	3Td+7Δt

FIG 8

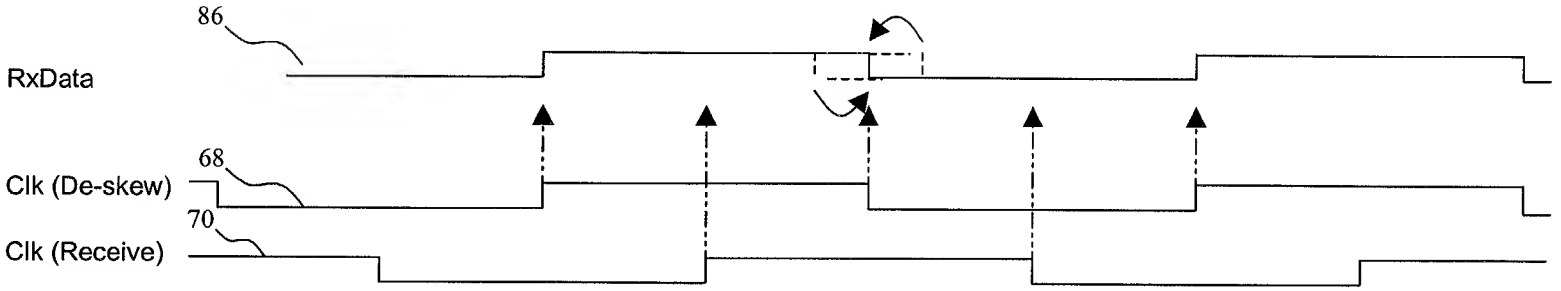

86
RxData
68
Clk (De-skew)
70
Clk (Receive)

FIG 9A

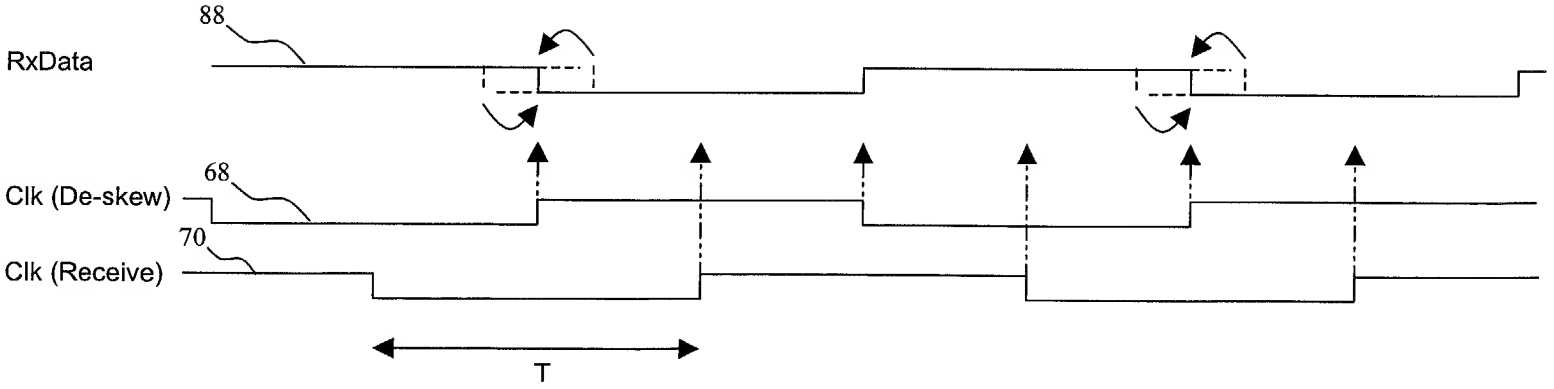

88
RxData
68
Clk (De-skew)
70
Clk (Receive)
T

FIG 9B

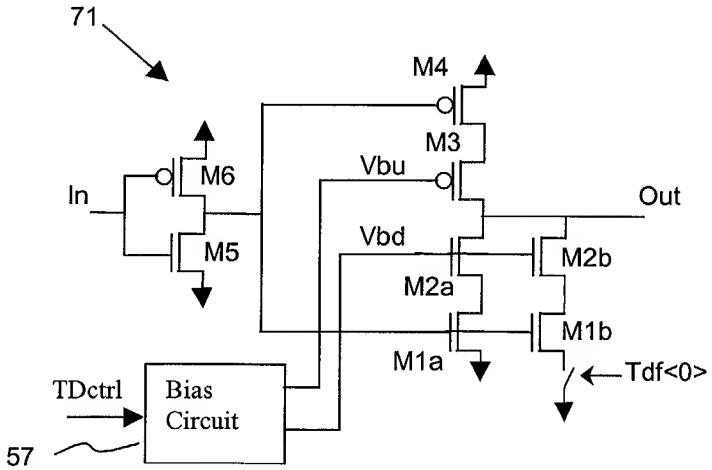

71
M4
M3
Vbu
M6
In
Out
Vbd
M5
M2b
M2a
M1b
M1a
Tdf<0>
TDctrl
Bias
Circuit
57

FIG 10

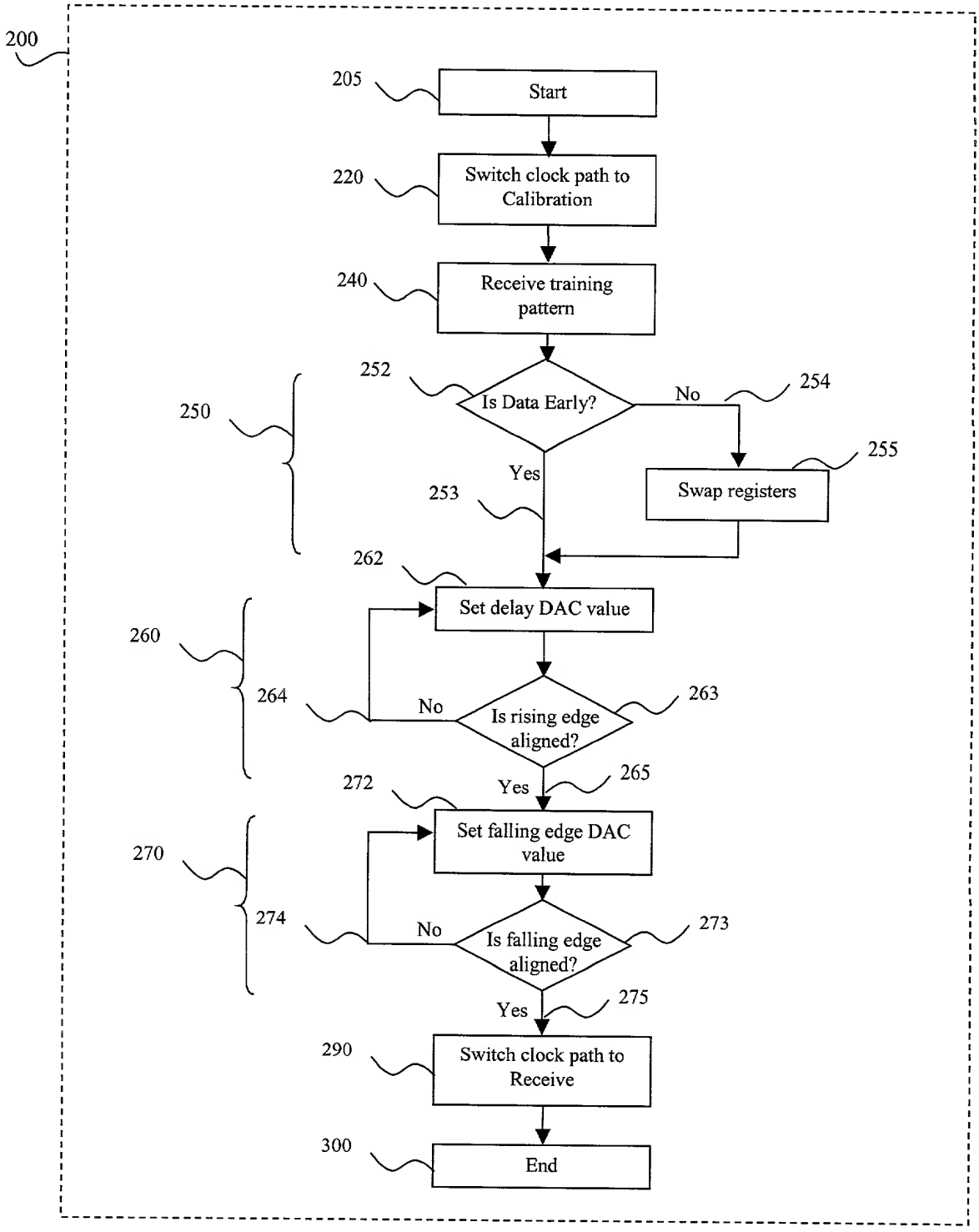

200
205
Start
220
Switch clock path to Calibration
240
Receive training pattern
252
Is Data Early?
No
254
250
255
Swap registers
Yes
253
262
Set delay DAC value
260
264
No
Is rising edge aligned?
263
Yes
265
272
Set falling edge DAC value
270
274
No
Is falling edge aligned?
273
Yes
275
290
Switch clock path to Receive
300
End

FIG 11